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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Bhakta et al.	Group Art Unit 2824
Appl. No.	:	11/862,931	
Filed	:	September 27, 2007	
For	:	MEMORY MODULE DECODER	
Examiner	:	Alexander Sofocleous	

PRELIMINARY AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Prior to examination on the merits, please amend the above-captioned application as described herein.

Amendments to the Claims: Begin on page 2 of this Preliminary Amendment

Remarks: Begin on page 10 of this Preliminary Amendment.

AMENDMENTS TO THE CLAIMS

Please cancel Claims 25-48 without prejudice.

Please add Claims 49-101 as indicated below.

1.-48. (Canceled)

49. (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register.

50. (New) The memory module of Claim 49, wherein the circuit is configured to store an input control signal of the set of input control signals during a row access procedure and to transmit the stored input control signal as an output control signal of the set of output control signals during a column access procedure.

51. (New) The memory module of Claim 49, wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals greater than the first number of chip-select signals.

52. (New) The memory module of Claim 51, wherein the first number of chip-select signals is two and the second number of chip-select signals is four.

53. (New) The memory module of Claim 49, wherein the circuit receives and buffers a plurality of row/column address signals of the input control signals during a row access procedure and sends the buffered plurality of row/column address signals to the plurality of DDR memory devices during a subsequent column access procedure.

54. (New) The memory module of Claim 49, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

55. (New) The memory module of Claim 49, wherein the bank address signals of the set of input control signals are received by both the logic element and the register.

56. (New) The memory module of Claim 49, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

57. (New) The memory module of Claim 49, wherein the register comprises a plurality of register devices.

58. (New) The memory module of Claim 49, wherein the plurality of DDR memory devices is arranged as a first set of DDR memory devices on a first side of the printed circuit board, a second set of DDR memory devices on the first side of the printed circuit board, a third set of DDR memory devices on a second side of the printed circuit board, and a fourth set of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the second set spaced from the DDR memory devices of the first set, the DDR memory devices of the fourth set spaced from the DDR memory devices of the third set.

59. (New) The memory module of Claim 58, wherein the DDR memory devices of the second set are spaced from the DDR memory devices of the first set in a direction along the first side and the memory devices of the fourth set are spaced from the memory devices of the third set in a direction along the second side.

60. (New) The memory module of Claim 49, wherein the plurality of DDR memory devices comprises a plurality of DDR2 memory devices arranged in a first rank, a second rank, a third rank, and a fourth rank, the first rank and the second rank on a first side of the printed circuit board, the third rank and the fourth rank on a second side of the printed circuit board, the second side different from the first side.

61. (New) The memory module of Claim 60, wherein the first rank is spaced from the second rank and the third rank is spaced from the fourth rank.

62. (New) The memory module of Claim 49, wherein the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density, the second memory density greater than the first memory density.

63. (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by

selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register.

64. (New) The memory module of Claim 63, wherein the command signal is transmitted to only one DDR memory device at a time.

65. (New) The memory module of Claim 64, wherein the command signal comprises a read command signal.

66. (New) The memory module of Claim 63, wherein the command signal is transmitted to two ranks of the first number of ranks at a time.

67. (New) The memory module of Claim 66, wherein the command signal comprises a refresh command signal.

68. (New) The memory module of Claim 66, wherein the command signal is transmitted to the two ranks of the first number of ranks concurrently.

69. (New) The memory module of Claim 63, wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure.

70. (New) The memory module of Claim 63, wherein the command signal comprises a read command signal or a write command signal, the set of input signals comprises a density bit which is a row address bit, and the circuit is configured to store the row address bit during an activate command for a selected bank.

71. (New) The memory module of Claim 63, wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure and to transmit the stored input signal as an output signal of the set of output signals during a subsequent column access procedure.

72. (New) The memory module of Claim 63, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

73. (New) The memory module of Claim 63, wherein the set of input signals comprises a plurality of row/column address signals received and buffered by the register and sent from the register to the plurality of DDR memory devices.

74. (New) The memory module of Claim 73, wherein the logic element receives the bank address signals and the command signal from the computer system and the register receives the bank address signals and the command signal from the computer system.

75. (New) The memory module of Claim 63, wherein two or more of the phase-lock loop device, the register, and the logic element are portions of a single component.

76. (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices coupled to the printed circuit board, the plurality of DDR DRAM devices having a first number of DDR DRAM devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising a row/column address signal, bank address signals, a chip-select signal, and an input command signal, the set of input control signals configured to control a second number of DDR DRAM devices arranged in a second number of ranks, the second number of DDR DRAM devices smaller than the first number of DDR DRAM devices, the second number of ranks smaller than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals comprising an output command signal, the set of output control signals configured to control the first number of DDR DRAM devices arranged in the first number of ranks, wherein the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks and transmitting the set of output control signals to at least one DDR DRAM device of the selected at least one rank; and

a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR DRAM devices, the logic element, and the register.

77. (New) The memory module of Claim 76, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device.

78. (New) The memory module of Claim 77, wherein the circuit is configured to store an input control signal of the set of input control signals during a row access procedure and to transmit the stored input control signal as an output control signal of the set of output control signals during a column access procedure.

79. (New) The memory module of Claim 76, wherein the set of input control signals comprises fewer chip-select signals than does the set of output control signals.

80. (New) The memory module of Claim 79, wherein the set of input control signals comprises two chip-select signals and the set of output control signals comprises four chip-select signals.

81. (New) The memory module of Claim 76, wherein the register receives the bank address signals and the input command signal of the set of input control signals.

82. (New) The memory module of Claim 76, wherein the first number of ranks is four and the second number of ranks is two.

83. (New) The memory module of Claim 76, wherein the first number of ranks is two and the second number of ranks is one.

84. (New) The memory module of Claim 76, wherein the input command signal is a refresh signal and the output command signal is a refresh signal.

85. (New) The memory module of Claim 76, wherein the input command signal is a precharge signal and the output command signal is a precharge signal.

86. (New) The memory module of Claim 76, wherein the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal.

87. (New) A memory module connectable to a computer system, the memory module comprising:

a printed circuit board having a first side and a second side;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, each DDR memory device comprising one or more banks, the plurality of DDR memory devices arranged in two or more ranks which are selectable by a first number of chip-select signals, the plurality of DDR memory devices comprising a first

rank of DDR memory devices on the first side and a second rank of DDR memory devices on the first side, the DDR memory devices of the second rank spaced from the DDR memory devices of the first rank; and

at least one integrated circuit element mounted to the printed circuit board, the at least one integrated circuit element receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals, the at least one integrated circuit element generating a plurality of output signals in response to the plurality of input signals, the plurality of output signals comprising row address signals, column address signals, bank address signals, command signals, and the first number of chip-select signals, the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank.

88. (New) The memory module of Claim 87, wherein the plurality of output signals corresponds to a first number of DDR memory devices arranged in the two or more ranks which are selectable by the first number of chip-select signals and wherein the plurality of input signals corresponds to a second number of DDR memory devices arranged in ranks which are selectable by the second number of chip-select signals, wherein the memory module simulates a virtual memory module having the second number of DDR memory devices.

89. (New) The memory module of Claim 87, wherein the at least one integrated circuit element comprises one or more integrated circuit elements selected from the group consisting of: an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, and a complex programmable-logic device.

90. (New) The memory module of Claim 87, wherein the at least one integrated circuit element comprises a logic element and a register.

91. (New) The memory module of Claim 90, wherein the row address signals and the column address signals of the plurality of input signals are received and buffered by the register and are sent from the register to the plurality of DDR memory devices.

92. (New) The memory module of Claim 91, wherein the logic element receives the second number of chip-select signals.

93. (New) The memory module of Claim 92, wherein both the register and the logic element receive the bank address signals and at least one command signal of the plurality of input signals.

94. (New) The memory module of Claim 90, wherein the at least one integrated circuit element further comprises a phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register.

95. (New) The memory module of Claim 94, wherein two or more of the logic element, the register, and the phase-lock loop device are portions of a single component.

96. (New) The memory module of Claim 87, wherein the plurality of DDR memory devices is arranged as the first rank of DDR memory devices on the first side of the printed circuit board, the second rank of DDR memory devices on the first side of the printed circuit board, a third rank of DDR memory devices on the second side of the printed circuit board, and a fourth rank of DDR memory devices on the second side of the printed circuit board, the DDR memory devices of the fourth rank spaced from the DDR memory devices of the third rank.

97. (New) The memory module of Claim 87, wherein the DDR memory devices of the second rank are spaced from the DDR memory devices of the first rank in a direction along the first side.

98. (New) The memory module of Claim 87, wherein the plurality of DDR memory devices comprises a plurality of DDR2 memory devices arranged in the first rank, the second rank, a third rank, and a fourth rank, the third rank and the fourth rank on the second side of the printed circuit board.

99. (New) The memory module of Claim 87, wherein the plurality of input signals corresponds to a first memory density, and the plurality of output signals corresponds to a second memory density, the second memory density greater than the first memory density.

100. (New) The memory module of Claim 87, wherein the at least one integrated circuit element is configured to respond to the plurality of input signals by selecting at least one rank of the two or more ranks and transmitting a command signal to at least one DDR memory device of the selected at least one rank.

101. (New) The memory module of Claim 87, wherein the at least one integrated circuit element is configured to store a signal of the plurality of input signals during a row access procedure and to transmit the stored signal as an output signal of the plurality of output signals during a column access procedure.

REMARKS

Claims 1-48 have been cancelled without prejudice and new Claims 49-101 have been added. Applicants believe that none of the foregoing amendments have added new matter to the application.

All of the claims currently pending in the present application are believed to be allowable over the prior art, and such action is earnestly solicited. If, however, any matters remain which could be resolved by Examiner's Amendment, the Examiner is cordially invited to contact the undersigned by telephone so that any such matters can be promptly resolved.

Respectfully submitted,

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Dated: June 22, 2009

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